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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/821,047	04/08/2004	Jente B. Kuang	AUS920040022US1	9651

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EXAMINER	
TAN, VIBOL	
ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 06/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/821,047	KUANG ET AL.	
	Examiner	Art Unit	
	Vibol Tan	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 April 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/8/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the first second and third potentials must be shown/labeled or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1, 3, 5, 20 and 22 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, line 4, it is not clear what applicant refers to as the domain output and a first output. Clarification is necessary.

Claims 1 and 20 recite "the first-cut inverter" in lines 10 and 15, respectively. There is insufficient antecedent basis for this limitation in the claim.

Claim 3 recites the limitation "the second logic state of a second control signal" in line 2 and "the first logic state of the second control signal" in line 3. There is insufficient antecedent basis for this limitation in the claim.

Claim 5 recites the limitation "the input of the first cut_inverter" in lines 2-3. There is insufficient antecedent basis for this limitation in the claim.

In claim 20, lines 9 and 10, it is not clear what applicant refers to as the domain output and a first output. Clarification is necessary.

Claim 22 recites the limitation "the second logic state of a second control signal" in line 2 and "the first logic state of the second control signal" in line 3. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Taguchi et al. (U. S. PAT. 5,557,221) in view of Toyoda et al. (U. S. PAT. 6,862,226).

In claim 1, Taguchi et al. teaches all claimed features in Fig. 1, an interface logic circuit for coupling a domain output of a first logic circuit domain (1) to a domain input of a second logic circuit domain (not shown) comprising: a first cut-circuit powered (34) by first and second voltage potentials (Vcc and ground) and having a first input coupled to the domain output (at P1), and a first output coupled to the domain input (input of the second logic circuit, not shown), wherein the first voltage potential (Vcc) is coupled to the first cut-circuit (34) in response to a first logic state (logic 0) of a first control signal (CONT SGL) and decoupled from the first cut-circuit in response to a second logic state (logic 1) of the first control signal; and a latch circuit (35) wherein the latch circuit latches logic states (logics 1 and 0) at the domain input when the first voltage potential is decoupled from the first cut-circuit; with the exception of teaching the latch circuit having a latch input coupled to the first input, and a latch output coupled to the first output. However, Toyoda et al. teaches in Fig. 1, a latch circuit (INV1 & INV2) having a latch input coupled to the first input (9), and a latch output coupled to the first output (10).

Therefore; it would have been obvious to one ordinary skill in the art at the time of the invention was made to combine the teachings of Taguchi et al. with the teachings of Toyoda et al. in order to provide an interface logic circuit which operates in an electrical stable manner, and when in normal operation operates at a high speed and low power consumption.

In claims 2 and 19, Taguchi et al. further teaches, the interface logic circuit of claim 1, wherein the latch circuit (35) is powered by the second voltage potential (ground) and a third voltage potential (another Vcc), and the third potential is coupled to the latch circuit in response to the second logic state (logic 1) of the first control signal (CONT SGL) and decoupled from the latch circuit in response to the first logic state (logic 0) of the first control signal; and wherein the first and third voltage potentials are equal (Vcc).

In claims 3 and 4, Taguchi et al. further teaches, the interface logic circuit of claim 2, wherein the second voltage potential (ground) is coupled to the first cut-circuit (34) in response to the second logic state (logic 1) of a second control signal (shown as same signal as CONT SGL) and decoupled from the first cut-circuit in response to the first logic state of the second control signal; and wherein the second voltage potential (ground) is coupled to the latch circuit (35) in response to the first logic state (logic 1) of the second control signal and decoupled from the latch circuit in response to the second logic state (logic 0) of the second control signal.

In claim 5, Taguchi et al. further teaches, the interface logic circuit of claim 1, wherein the first cut-circuit comprises: an inverter stage (36, 37) having an inverter input (as shown) coupled as the input of the first cut-inverter, an inverter output coupled as the output of the first cut-inverter, a first power supply node (Vcc), and a second power supply node coupled to the second voltage potential (ground); and a first electronic switch (38) coupling the first voltage potential to the first power supply node in response to the first logic state (logic 0) of the first control signal and decoupling the first voltage

potential from the first power supply node in response to the second logic state (logic 1) of the first control signal.

Claims 6-18 correspond to detailed circuitry already discussed similarly with regard to claims 1-5.

6. Claims 20- 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tobin et al. (U. S. PAT. 6,275,077) in view of Taguchi et al. and further in view of Toyoda et al.

In claim 20, Tobin et al. teaches all claimed features in Fig. 15, a data processing system comprising: a central processing unit (1502); a random access memory (1504); an input output (1506) interface unit; and a bus (not labeled) for coupling the CPU, RAM and I/O interface unit, the CPU having first and second logic circuit domains (inside 1502) and an interface logic circuit (1508) for coupling a domain output from the first logic circuit domain to a domain input to the second logic circuit domain; with the exception of teaching the details of the interface circuit. However, Taguchi et al. teaches in Fig. 1, an interface circuit including a first cut-circuit (34) powered by first and second voltage potentials (Vcc and ground) and having a first input coupled to the domain output (at P1), and a first output coupled to the domain input (a circuit coupled after 49, not shown), wherein the first voltage potential is coupled to the first cut-circuit in response to a first logic state (logic 0) of a first control signal (CONT SGL) and decoupled from the first cut-circuit in response to a second logic state (Logic 1) of the first control signal, and a latch circuit (35) with the exception of teaching the latch circuit having a latch input coupled to the first input, and a latch output coupled to the first

output. However, Toyoda et al. teaches in Fig. 1, a latch circuit (INV1 & INV2) having a latch input coupled to the first input (9), and a latch output coupled to the first output (10).

Therefore; it would have been obvious to one ordinary skill in the art at the time of the invention was made to combine the teaching of Tobin et al. with the teachings of Taguchi et al. and further with the teachings of Toyoda et al. in order to provide an interface logic circuit which operates in an electrical stable manner, and when in normal operation operates at a high speed and low power consumption for a data processing system.

In claims 21 and 24, Taguchi et al. further teaches, the data processing of claim 1, wherein the latch circuit (35) is powered by the second voltage potential (ground) and a third voltage potential (another Vcc), and the third potential is coupled to the latch circuit in response to the second logic state (logic 1) of the first control signal (CONT SGL) and decoupled from the latch circuit in response to the first logic state (logic 0) of the first control signal; and wherein the first and third voltage potentials are equal (Vcc).

In claims 22 and 23, Taguchi et al. further teaches, the data processing of claim of claim 2, wherein the second voltage potential (ground) is coupled to the first cut-circuit (34) in response to the second logic state (logic 1) of a second control signal (shown as same signal as CONT SGL) and decoupled from the first cut-circuit in response to the first logic state of the second control signal; and wherein the second voltage potential (ground) is coupled to the latch circuit (35) in response to the first logic

state (logic 1) of the second control signal and decoupled from the latch circuit in response to the second logic state (logic 0) of the second control signal.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vibol Tan whose telephone number is (571) 272-1811. The examiner can normally be reached on Monday-Friday (7:00 AM-4:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike J. Tokar can be reached on (571) 272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

VIBOL TAN
PRIMARY EXAMINER